What is claimed is:

1. A boosting voltage control circuit, comprising:

in order to constantly keep a level of a voltage boosted by a pump,

a boosting voltage dividing means for dropping a boosting voltage;

a package voltage generating means for generating package voltage signals of various voltage levels depending on external trim bits;

a compare reference voltage generating means for generating a reference voltage and a control voltage according to the package voltage signal from the package voltage generating means;

a compare means driven by a control voltage, for comparing the dropped boosting voltage and the reference voltage to output a compare result signal;

an output means for outputting first and second clock control signals using the compare result signal from the compare means;

a clock generator for generating clock signals according to the first and second clock control signals; and

a first pump for always outputting the boosting voltage according to the clock signal and a second pump for outputting the boosting voltage according to an external read signal and the clock signal.

2. The boosting voltage control circuit as claimed in claim 1, wherein the package voltage generating means comprises:

a trim bit input unit for using first through third trim bit signals to

generate first through fourth voltage level control signals and first and second path control signals;

a voltage level converting unit for generating the package voltage signals having first through seventh voltage levels according to the first through fourth voltage level control signals and the first and second path control signals; and

a package voltage output unit for outputting the package voltage signals to the compare reference voltage generating means.

3. The boosting voltage control circuit as claimed in claim 2, wherein the trim bit input unit comprises:

a first inverter connected to a first trim bit input terminal, for inverting the first trim bit signal;

a second inverter connected to a second trim bit input terminal, for inverting the second trim bit signal;

a first NAND gate connected to the first and second inverters, for logically combining the inverted first and second trim bit signals to generate a first voltage level control signal;

a second NAND gate connected to the second inverter and the first trim bit input terminal, for logically combining the inverted second trim bit signal and the first trim bit signal to generate a second voltage level control signal;

a third NAND gate connected to the first inverter and the second trim bit input terminal, for logically combining the inverted first trim bit signal and the second trim bit signal to generate a third voltage level control signal;

a fourth NAND gate connected to the first and second trim bit input terminals, for logically combining the first and second trim bit signals to generate a fourth voltage level control signal;

a third inverter connected to the third trim bit input terminal, for inverting the third trim bit signal to generate the first path control signal; and

a fourth inverter connected to the third inverter, for inverting the first path control signal to generate the second path control signal.

4. The boosting voltage control circuit as claimed in claim 2, wherein the voltage level converting unit comprises:

a first PMOS transistor connected between the power supply voltage and a first node and driven by the second path control signal;

a second PMOS transistor connected between the power supply voltage and a second node and driven by the first path control signal;

a third PMOS transistor connected between the second node and a third node and driven by the third voltage level control signal;

a fourth PMOS transistor connected between the second node and a fourth node and driven by the second voltage level control signal;

a fifth PMOS transistor connected between the second node and a fifth node and driven by the first voltage level control signal;

a sixth PMOS transistor connected between the second node and the third node and driven by a sixth node;

a seventh PMOS transistor connected between the third node and the fourth node and driven by the sixth node;

an eighth PMOS transistor connected between the fourth node and the fifth node and driven by the sixth node;

a ninth PMOS transistor connected between the fifth node and the sixth node and driven by the sixth node;

a tenth PMOS transistor driven by the first voltage level control signal and eleventh and twelfth PMOS transistors driven by the sixth node, which are serially connected between the first node and the sixth node;

a thirteenth PMOS transistor connected between the first node and a seventh node and driven by the second voltage level control signal;

fourteenth and fifteenth PMOS transistors serially connected between the sixth node and the seventh node and driven by the sixth node;

sixteenth and seventh PMOS transistors serially connected between the sixth node and the seventh node and driven by the sixth node;

an eighteenth PMOS transistor connected between the first node and an eighth node and driven by the third voltage level control signal;

nineteenth twentieth PMOS transistors serially connected between the sixth node and the eighth node and driven by the sixth node;

twenty-first and twenty second PMOS transistors serially connected between the sixth node and the eighth node and driven by the sixth node;

twenty-third and twenty-fourth PMOS transistors serially connected between the sixth node and the eighth node and driven by the sixth node;

a twenty-fifth PMOS transistor connected between the first node and the ninth node and driven by the fourth voltage level control signal;

twenty-sixth and twenty-seventh PMOS transistors connected between

the sixth node and a ninth node and driven by the sixth node;

twenty-eighth and twenty-ninth PMOS transistors connected between the sixth node and the ninth node and driven by the sixth node;

thirtieth and thirty-first PMOS transistors connected between the sixth node and the ninth node and driven by the sixth node;

thirty-second and thirty-third PMOS transistors connected between the sixth node and the ninth node and driven by the sixth node; and

a thirty-fourth PMOS transistor connected between the first node and the sixth node and driven by the sixth node.

5. The boosting voltage control circuit as claimed in claim 1, wherein the boosting voltage dividing means comprises first through sixth PMOS transistors which are serially connected between the input terminal of the boosting voltage and the ground, wherein a source terminal and a gate terminal of each of the first through sixth PMOS transistors are connected.

6. The boosting voltage control circuit as claimed in claim 1, wherein the compare reference voltage generating unit comprises:

a PMOS transistor connected between the power supply voltage and the first node and driven by the package voltage signal;

a first NMOS transistor connected between the first node and the second node and driven by the first node; and

a second NMOS transistor connected between the second nod and the ground and driven by the second node.

7. A boosting voltage control circuit having a pump for transferring a pumped voltage, as an output, according to the output signal of a clock generator, and a regulation block for detecting a voltage of the output to control the clock generator, being characterized in that the regulation block comprises:

a boosting voltage dividing means for dropping a voltage of the output to a given level;

a package voltage generating means for generating package voltage signals of various voltage levels according to external trim bits;

a compare reference voltage generating means for generating a reference voltage and a control voltage according to the package voltage signal; and

a compare means for comparing the output of the voltage dividing means and the reference voltage according to the control voltage to generate a control signal for controlling the clock generator.

8. The boosting voltage control circuit as claimed in claim 7, wherein the package voltage generating means comprises:

a trim bit input unit for using first through third trim bit signals to generate first through fourth voltage level control signals and first and second path control signals;

a voltage level converting unit for generating the package voltage signals having first through seventh voltage levels according to the first ~

fourth voltage level control signals and the first and second path control signals; and

a package voltage output unit for outputting the package voltage signals to the compare reference voltage generating means.

9. The boosting voltage control circuit as claimed in claim 8, wherein the trim bit input unit comprises:

a first inverter connected to a first trim bit input terminal, for inverting the first trim bit signal;

a second inverter connected to a second trim bit input terminal, for inverting the second trim bit signal;

a first NAND gate connected to the first and second inverters, for logically combining the inverted first and second trim bit signals to generate a first voltage level control signal;

a second NAND gate connected to the second inverter and the first trim bit input terminal, for logically combining the inverted second trim bit signal and the first trim bit signal to generate a second voltage level control signal;

a third NAND gate connected to the first inverter and the second trim bit input terminal, for logically combining the inverted first trim bit signal and the second trim bit signal to generate a third voltage level control signal;

a fourth NAND gate connected to the first and second trim bit input terminals, for logically combining the first and second trim bit signals to generate a fourth voltage level control signal;

a third inverter connected to the third trim bit input terminal, for

inverting the third trim bit signal to generate the first path control signal; and

a fourth inverter connected to the third inverter, for inverting the first path control signal to generate the second path control signal.

10. The boosting voltage control circuit as claimed in claim 8, wherein the voltage level converting unit comprises:

a first PMOS transistor connected between the power supply voltage and a first node and driven by the second path control signal;

a second PMOS transistor connected between the power supply voltage and a second node and driven by the first path control signal;

a third PMOS transistor connected between the second node and a third node and driven by the third voltage level control signal;

a fourth PMOS transistor connected between the second node and a fourth node and driven by the second voltage level control signal;

a fifth PMOS transistor connected between the second node and a fifth node and driven by the first voltage level control signal;

a sixth PMOS transistor connected between the second node and the third node and driven by a sixth node;

a seventh PMOS transistor connected between the third node and the fourth node and driven by the sixth node;

an eighth PMOS transistor connected between the fourth node and the fifth node and driven by the sixth node;

a ninth PMOS transistor connected between the fifth node and the sixth node and driven by the sixth node;

a tenth PMOS transistor driven by the first voltage level control signal and eleventh and twelfth PMOS transistors driven by the sixth node, which are serially connected between the first node and the sixth node;

a thirteenth PMOS transistor connected between the first node and a seventh node and driven by the second voltage level control signal;

fourteenth and fifteenth PMOS transistors serially connected between the sixth node and the seventh node and driven by the sixth node;

sixteenth and seventh PMOS transistors serially connected between the sixth node and the seventh node and driven by the sixth node;

an eighteenth PMOS transistor connected between the first node and an eighth node and driven by the third voltage level control signal;

nineteenth twentieth PMOS transistors serially connected between the sixth node and the eighth node and driven by the sixth node;

twenty-first and twenty second PMOS transistors serially connected between the sixth node and the eighth node and driven by the sixth node;

twenty-third and twenty-fourth PMOS transistors serially connected between the sixth node and the eighth node and driven by the sixth node;

a twenty-fifth PMOS transistor connected between the first node and the ninth node and driven by the fourth voltage level control signal;

twenty-sixth and twenty-seventh PMOS transistors connected between the sixth node and a ninth node and driven by the sixth node;

twenty-eighth and twenty-ninth PMOS transistors connected between the sixth node and the ninth node and driven by the sixth node;

thirtieth and thirty-first PMOS transistors connected between the sixth

node and the ninth node and driven by the sixth node;

thirty-second and thirty-third PMOS transistors connected between the sixth node and the ninth node and driven by the sixth node; and

a thirty-fourth PMOS transistor connected between the first node and the sixth node and driven by the sixth node.

11. The boosting voltage control circuit as claimed in claim 7, wherein the boosting voltage dividing means comprises first through sixth PMOS transistors which are serially connected between the input terminal of the boosting voltage and the ground, wherein a source terminal and a gate terminal of each of the first through sixth PMOS transistors are connected.

12. The boosting voltage control circuit as claimed in claim 7, wherein the compare reference voltage generating unit comprises:

a PMOS transistor connected between the power supply voltage and the first node and driven by the package voltage signal;

a first NMOS transistor connected between the first node and the second node and driven by the first node; and

a second NMOS transistor connected between the second nod and the ground and driven by the second node.